REMARKS/ARGUMENTS

Applicants respectfully request reconsideration of the application as amended. Claims 10-18 are pending. Claims 10, 13, and 16 have been amended.

1. Response to § 102 Rejections

Claims 10, 12-13, 15-16 and 18 are rejected under 35 U.S.C. §102(b) as being anticipated by Ajanovic, et al. (U.S. Patent No. 5,761,444).

Ajanovic is directed at method and apparatus for regulating the deferral of a transaction issued on a bus by a processor (Ajanovic, Abstract). In Ajanovic, a transaction processor operates to defer the current transaction when there is a pending CPU bus transaction waiting to be issued and when the current CPU bus transaction is a candidate for deferral. (Ajanovic, 5: 1-7.) Specifically, when a pending CPU bus transaction is waiting to be processed on the data bus of the CPU bus and the current transaction is a candidate for deferral, transaction processor sends a signal to start CPU latency timer. CPU latency timer operates to define the amount of time given to the current transaction to complete before it is deferred *in the presence of another pending transaction*. (Ajanovic, 5: 25-31.)

Thus, *the latency timer in Ajanovic is not started unless another transaction is present* (Ajanovic, Figure 7). In other words, the starting of the timer Ajanovic is responsive to detecting another pending transaction, rather than responsive to the dispatching of the current transaction. This is distinct from "starting a timer **in response to dispatching** of the bus transaction," as recited in claims 1 and 16, as amended.

Because Ajanovic fails to disclose or suggest each and every element of claims 1 and 16, claims 1, 16, and their respective dependent claims are patentable and should be allowed.

Claim 13, as amended, recites "a timer coupled to the detector, the timer to start in response to dispatching of the command." Thus, claim 13 is patentable and should be allowed for at least the reasons articulated with respect to claims 1 and 16.

2. Response to § 103 Rejections

Claims 11, 14 and 17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ajanovic, et al. (U.S. Patent No. 5,761,444) in view of Ljunberg, et al. (U.S. Patent No. 5,493,566).

Claims 11, 14, and 17 include the features of claims 1, 12, and 17 respectively, by virtue of their being dependent on those claims. Ljungberg is directed at a system for controlling the flow of data cells through a packet switch (Ljungberg, Abstract). Ljungberg, whether considered separately or in combination with Ajanovic, fails to disclose or suggest "starting a timer in response to dispatching of the bus transaction" as required by claims 1 and 17 by virtue of their being dependent on claims 1 and 16 respectively. Ljungberg, whether considered separately or in combination with Ajanovic, also, fails to disclose or suggest "starting a timer in response to dispatching of the bus transaction" as required by claim 13 by virtue of its being dependent on claim 13.

Thus, 11, 14, and 17 are patentable in view of Ljungberg and Ajanovic combination for at least the reasons articulated with respect to claims 1, 13, and 16.

Furthermore, the Office action correctly states that Ajanovic does not expressly teach "wherein starting occurs only if an in-order-queue has a depth of 1." The Office action therefore combined Ajanovic with Ljungberg in an attempt to show this feature. Specifically, the Office action cited the following portion of Ljungberg:

> In an ATM switch constructed in accordance with the principles of the present invention, the fullness of the output buffers 75 in the switch core 67 is constantly monitored by a device such as a half-full flag. If the content of an output buffer exceeds a threshold value, this is detected. Such observations related to the status of the output buffers are signaled continuously to the access devices 73 associated with each switch port 74 whether such access devices are located internally or externally to the switch ports. In this manner, the access devices 73 always have relevant

> information concerning those output buffers 75 which contain a large amount of data, i.e., are in danger of becoming overfull with the consequent loss of data cells. The access devices 73 utilize the output buffer status reports 57 to inhibit transmission of that traffic which is destined to those output buffers 75 which have the highest loads. Those data cells are retained in the input buffers 71.
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> Ljungberg, 6: 31-48.

As is evident from the passage above, there is no reference to an in-order queue having a depth of 1," as recited in claims 11, 14, and 17. This feature is not disclosed anywhere else in Ljungberg either. Because Ljungberg, whether considered separately or in combination with Ajanovic, fails to disclose or suggest each and every element of claims 11, 14, and 17, claims 11, 14, and 17 are patentable in view of Ljungberg and Ajanovic combination and should be allowed.

3. Conclusion

Having tendered the above remarks and amended the claims as indicated herein, Applicants respectfully submit that all rejections have been addressed and that the claims are now in a condition for allowance, which is earnestly solicited.

If there are any additional fees due in connection with this communication, please charge our deposit account no. 02-2666. If a telephone interview would in any way expedite the prosecution of the present application, the Examiner is invited to contact Elena Dreszer at (408) 720-8300.

Respectfully submitted,
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